## IN THE CLAIMS

Please cancel Claims 12-17 without prejudice or disclaimer.

Claim 1 (currently amended): An amplifier circuit, comprising:

a first stage and a second stage, the first stage comprising a quad configuration having all NPN devices and the second stage comprising a translinear current amplifier configuration; and

a coupling circuit operably coupling the first stage and the second stage ~~to reduce transistor beta loading effects~~.

Claim 2 (original): The amplifier circuit recited in Claim 1, wherein the first stage quad configuration is modified using emitter degeneration.

Claim 3 (original): The amplifier circuit recited in Claim 1, wherein the current gain of the second stage is given by:

$$(I A_{out\ 1} - I A_{out\ 2})/(I_{out1} - I_{out2}) = (1 + R_{123} / R_{124}) \cdot (I_{135} / I_{134}) \cdot (A / (1+A))$$

where $A = g_{m\ Q109} \cdot R_{124}$;

$IA_{out1}$ is the amplified output collector current from $Q_{110}$;

$IA_{out2}$ is the output collector current from transistor $Q_{111}$;

$I_{out1}$ is the output current from $Q_{103}$ and $Q_{105}$ from the first stage quad, and $I_{out2}$ is the collector current from $Q_{104}$ and $Q_{106}$ from the first stage quad;

$R_{123}$ is the resistance value of the third resistor and $R_{124}$ is the resistance value of the fourth resistor;

$I_{135}$ is the current through the fifth current source; and

$I_{134}$ is the value of the current through the fourth current source.

Claim 4 (original): The amplifier circuit recited in Claim 1, further comprising current to voltage conversion and common mode feedback in the second stage operable to provide high speed, low distortion and extended bandwidth.

Claim 5 (currently amended): The amplifier circuit recited in Claim 1, wherein the amplifier is formed of ~~complementary~~ bipolar devices.

Claim 6 (original): The amplifier circuit recited in Claim 1 being adapted for use in an integrated circuit.

Claim 7 (original): The amplifier circuit recited in Claim 1 being adapted for use in a variable gain amplifier.

Claim 8 (currently amended): An amplifier circuit, comprising a first stage and a second stage, the first stage comprising a quad configuration having all NPN devices, and the second stage comprising a resistive shunt current feedback amplifier with a Darlington/level shift input stage ~~operable to reduce transistor beta loading effects~~.

Claim 9 (original): The amplifier circuit recited in Claim 8, wherein the first stage quad is modified using emitter degeneration.

Claim 10 (currently amended): An amplifier circuit, comprising:

a first stage quad operable to bias transistors having all NPN devices; and

a coupling circuit coupling the first stage quad to a second stage translinear current amplifier operable to ~~reduce transistor beta loading effects and~~ provide improved slew rate, low distortion and extended bandwidth.

Claim 11 (original): The amplifier circuit recited in Claim 10, wherein the first stage quad is modified using emitter degeneration.

Claims 12-17 (cancelled)